EEE646 FPGA BASED SYSTEM DESIGN

Slot :G1+TG1

L	T	P	C
3	0	0	3

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Outline

- Course Objective & Outcomes
- Syllabus
- Evaluation Procedure
- Integrated Circuit – An Overview & Evolution
- VLSI- Device Perspective
- VLSI-System Perspective
- Typical IC Design Flow
- Integrated Circuit Food Chain
- Discussion

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Objective and Outcomes

Objective of the Course:

This course covers the advanced design and analysis of digital circuits with HDL. The primary goal is to provide in depth understanding of system design. The course enables students to apply their knowledge for the design of advanced digital hardware systems with help of FPGA tools.

Course Outcomes

Upon successful completion of this course, students will be able to:

1. Design and optimize complex combinational and sequential digital circuits
2. Model combinational and sequential digital circuits by Verilog HDL
3. Design and model digital circuits with Verilog HDL at behavioral, structural, and RTL Levels
4. Develop test benches to simulate combinational and sequential circuits.
5. Understand the FPGA Architecture

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Syllabus

Unit I Verilog HDL Coding Style:

Lexical Conventions - Ports and Modules – Operators - Gate Level Modeling - System Tasks &Compiler Directives - Test Bench - Data Flow Modeling - Behavioral level Modeling -Tasks & Functions.

Unit II Verilog Modeling of Combinational & Sequential Circuits:

Behavioral, Data Flow and Structural Realization – Adders – Multipliers- Comparators - Flip Flops - Realization of Shift Register - Realization of a Counter- Synchronous and Asynchronous FIFO –Single port and Dual port RAM – Pseudo Random LFSR – Cyclic Redundancy Check.

Unit III Synchronous Sequential Circuit:

State diagram-state table –state assignment-choice of flip-flops – Timing diagram –One hot encoding-Mealy and Moore state machines – Design of serial adder using Mealy and Moore state machines - State minimization – Sequence detection- Design of vending machine using One Hot Controller

Unit IV FPGA and its Architecture:

Types of Programmable Logic Devices- PLA & PAL- FPGA Generic Architecture. ALTERA Cyclone II Architecture – Timing Analysis and Power analysis using Quartus-II- SOPC Builder- NIOS-II Soft-core Processor- System Design Examples using ALTERA FPGAs – Traffic light Controller, Real Time Clock - Interfacing using FPGA: VGA, Keyboard, LCD.

Text book / References

- Samir Palnitkar, “Verilog HDL: A Guide to Digital Design and Synthesis” Prentice Hall, Second Edition, 2003.
- T.R.Padmanabhan, B.Bala Tripura Sundari, “Design through Verilog HDL” Wiley Interscience, 2004.
- S. Ramachandran, “Digital VLSI System Design: A Design Manual for implementation of Projects on FPGAs and ASICs Using Verilog” Springer Publication, 2007.
- Wayne Wolf , “FPGA Based System Design”, Prentices Hall Modern Semiconductor Design Series.
- Stephen Brown & Zvonko Vranesic, “Digital Logic Design with VerilogHDL” TATA McGraw Hill Ltd. 2nd Edition 2007.
- SOPC & NIOS II Online Tutorial www.altera.com

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Mode of Evaluation

Component	Marks	Weightage	Tentative Date
Assessment Test	50	20	16th -23rd August
Surprise Test	10	10	After Assessment Test
Project	20	25	3rd to 11th October
Term end Exam	100	45	16th Nov – 3rd Dec
	Total	100	

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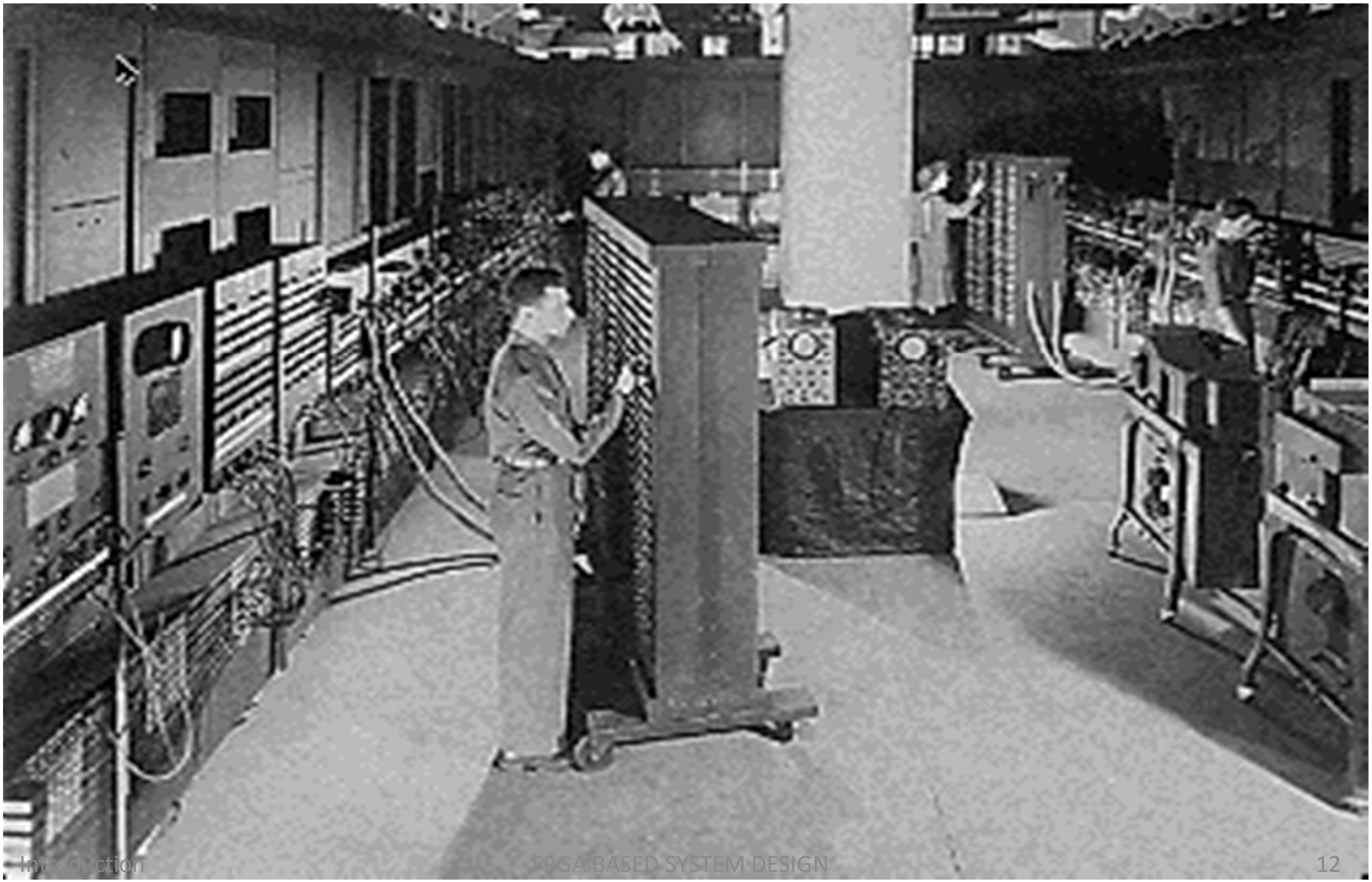
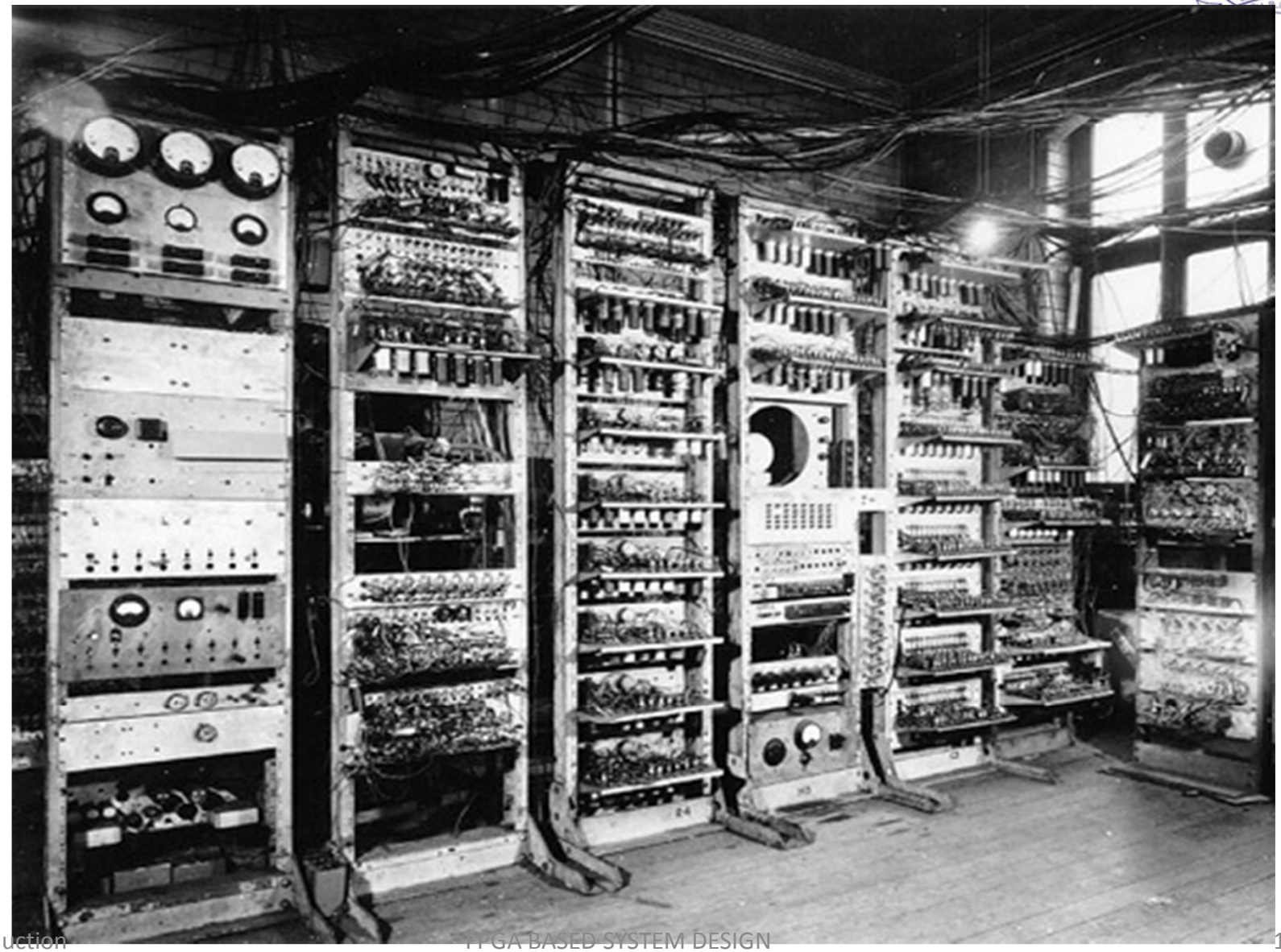
Integrated Circuit – An Overview & Evolution

Picture of Part of ENIAC (Electronic Numerical Integrator And Calculator)



ENIAC FROM ANOTHER ANGLE



ENIAC vs. Microcomputer

ENIAC

- **Size : 30 x 50 ft**
- **Weight : 30 tons**
- **Tubes : 18 K**
- **Resistors: 70 K**
- **Capacitors : 10 K**
- **Switches : 6 K**
- **Power : 150 kW**
- **Cost (1940) : US $ 400 K**

Microcomputer

- **Size : ¼ inch x ¼ inch**
- **Weight : nil**
- **Power < light bulb**
- **Speed : 20 times faster**
- **Memory : larger, more computing capacity**
- **Cost < $300 (*compare with $ 400 K + inflation over 34 years).***

Miniaturization: December 23, 1947

From left: Bardeen, Shockley, Brattain

Nobel Winners of Physics in 1956

First Point Contact Transistor of Bardeen and Brattain

Dawn of the transistor

Bell Labs lays the groundwork:

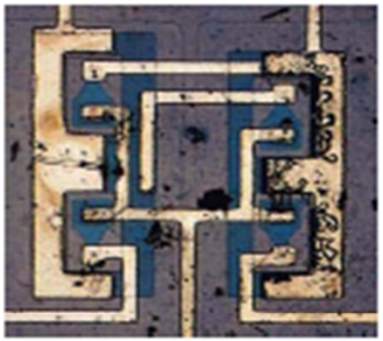
1940: Russel Ohl develops PN junction which produces 0.5V when exposed to light.

1945: Bell sets up lab in the hopes of developing "solid state" components to replace existing electromechanical systems. William Schockley, John Bardeen, Walter Brattain: all solid-state physicists. Focus on Si and Ge.

1947: Bardeen and Brattain create point-contact transistor w/ two PN junctions. Gain = 18.

Announced in July 1948. But treated as a novelty until 1951 invention of junction transistor. Bell Labs willing to license the rights to the transistor to any company for a royalty (which was waived for hearing aid companies as a gesture to Alex. G. Bell). Transistor was good: smaller, faster, more reliable and economical but this is only half the story since the circuits, albeit smaller, were still constructed in much the same way.

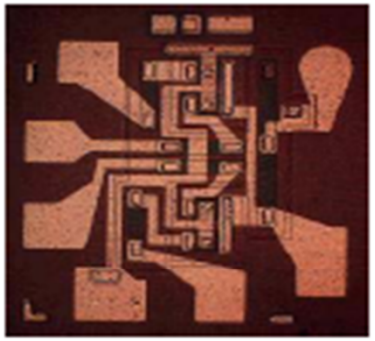
1960's: era of integration (social and electrical!)



0.06"

1961: TI and Fairchild introduced the first logic IC's (cost ~$50 in quantity!). This is a dual flip-flop with 4 transistors.

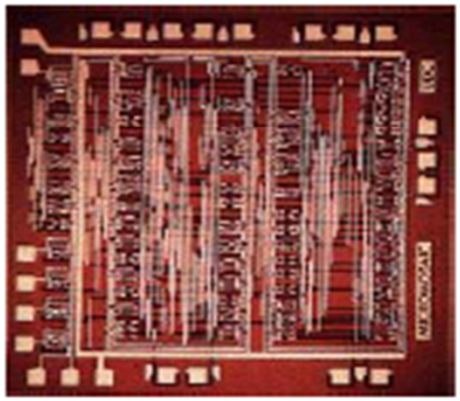
1963: Densities and yields are improving. This circuit has four flip flops.



0.038"

1966: Robert Dennard invents 1-T DRAM at IBM TJ Watson Research Center.

1967: Fairchild markets this semi-custom chip. Transistors (organized in columns) could be easily rewired using a two-layer interconnect to create different circuits. This circuit contains ~150 logic gates. Masks are laid-out, cut and checked by hand... beginnings of a design flow but no computer automation.



0.15"

Levels of Integration

- Small Scale Integration (<10 Transistors)
- Medium Scale Integration (<1000 Transistors)
- Large Scale Integration (<10000 Transistors)
- Very Large Scale Integration(> million Transistors)
- Giga Scale Integration (> billion Transistors)

What is a VLSI circuit?

VERY LARGE SCALE INTEGRATED CIRCUIT

Technique where many circuit components and the wiring that connects them are manufactured simultaneously into a compact, reliable and inexpensive chip.

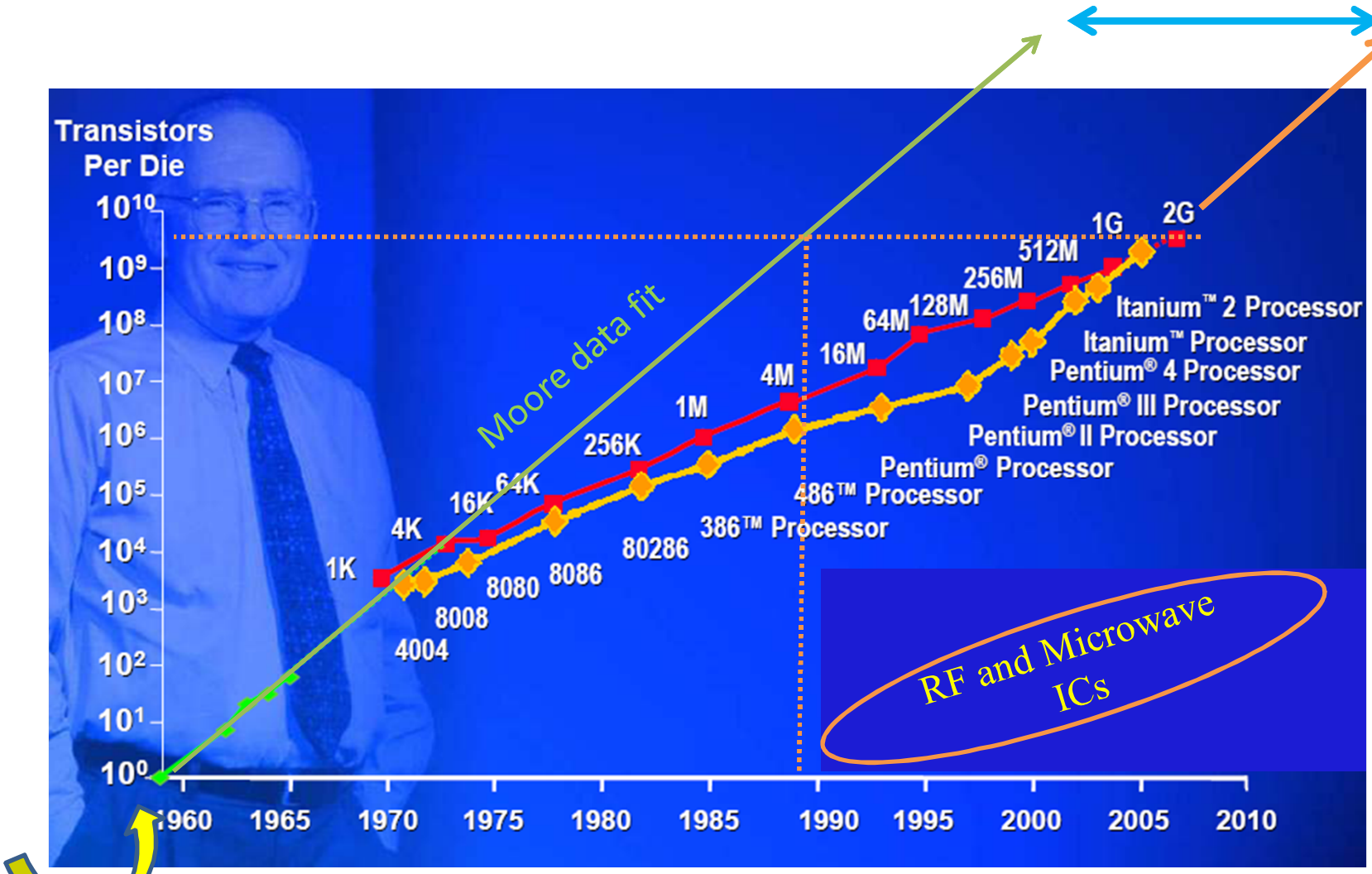
Early (circa 1977) characterization of circuit "size" before people realized that the number of components per chip was quadrupling every 24 months (aka Moore's Law)!

Trends in Integrated Circuits

- Reduce the device geometry (Scaling)
- more circuit blocks in a chip (Processors)
- higher speed (Novel devices)
- low power consumption (Silicon Technology)

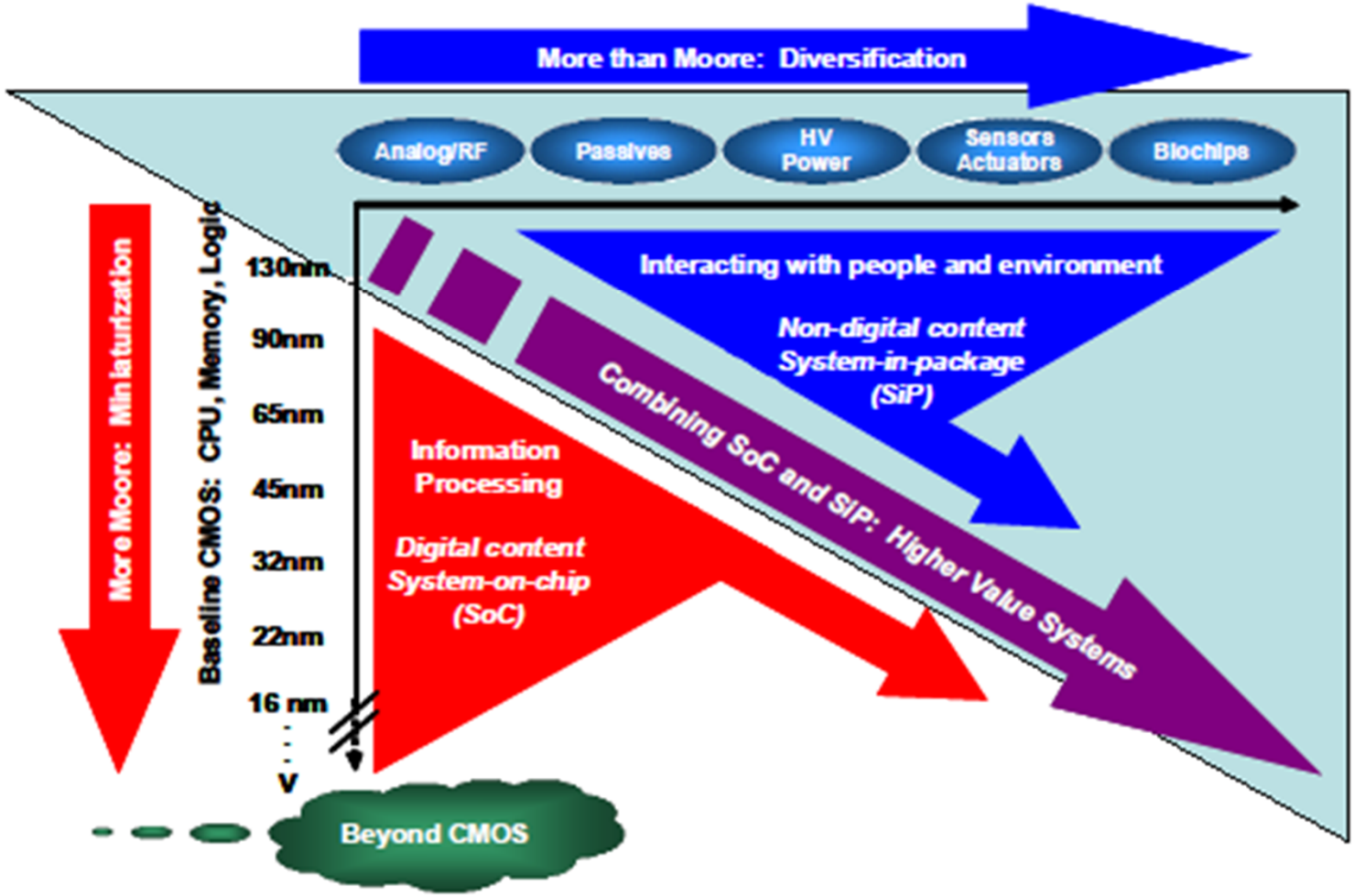
Moore's law

Size of the device
Fabrication complexity
Device Reliability



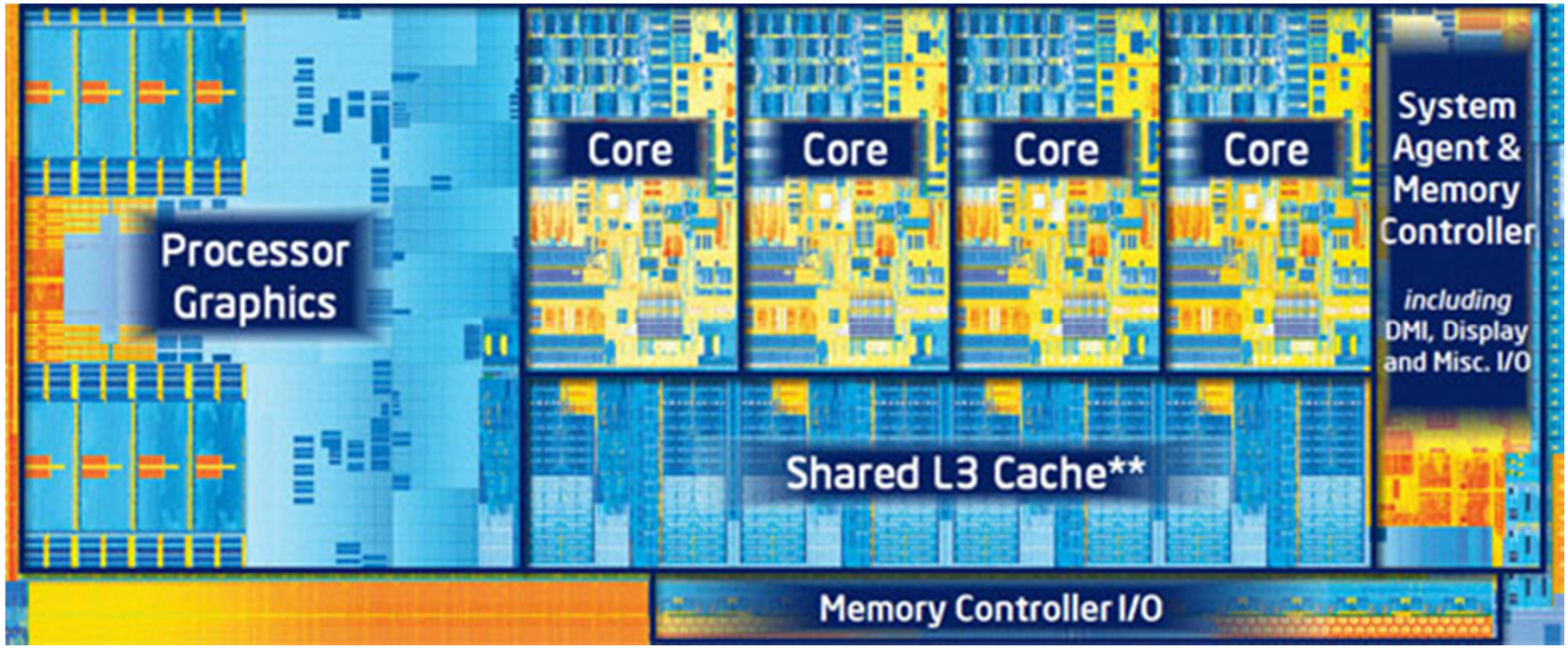
Source: Intel

More Moore & More than Moore



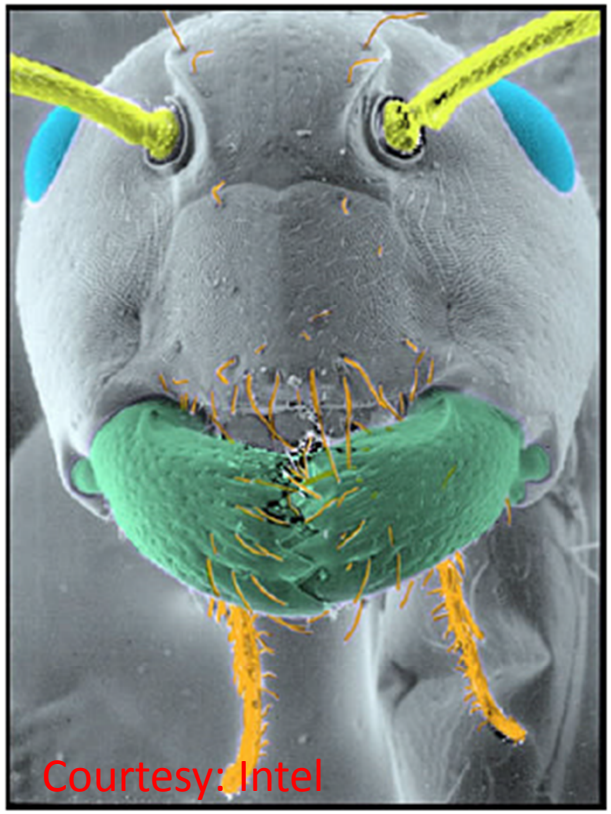
[ITRS, 2011]

Intel Core i7-3770K



1.4 billion transistors

Another Perspective on Moore's Law



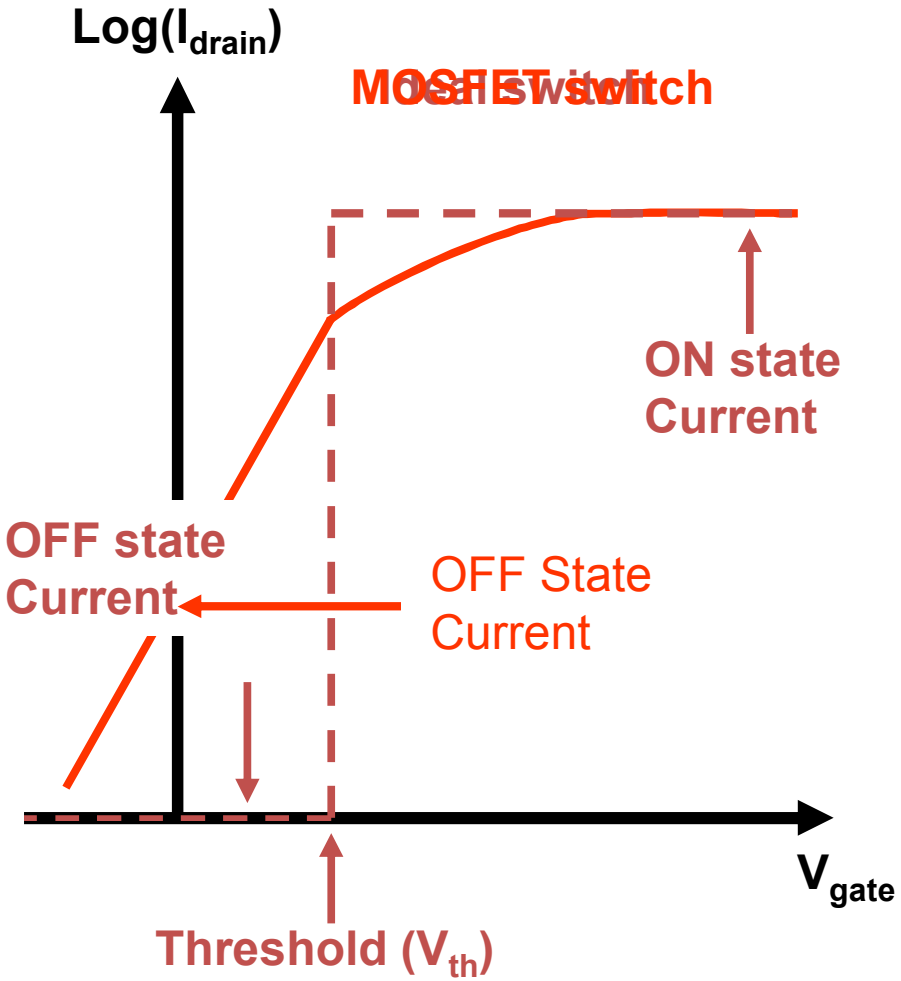
… we are already producing 10^{18} transistors per year. Enough to supply every ant on the planet with ten transistors.

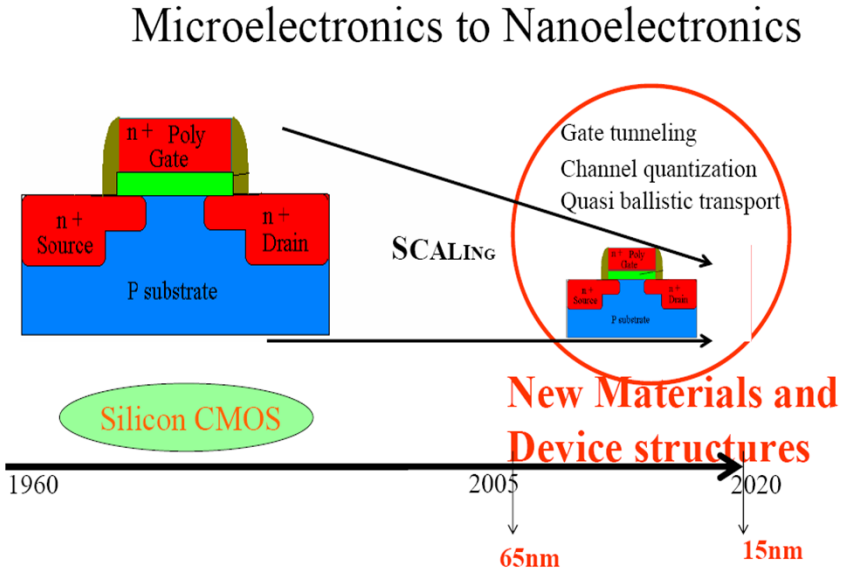
Twenty years from now, if the trend continues, there will be more transistors than there will be cells in the total number of human bodies on Earth.

Why Scaling?

- Technology shrinks by 0.7/generation
- With every generation can integrate 2x more functions per chip for about the same $/chip
- Cost of a function decreases by 2x
- But …
  - How to design chips with more and more functions?
  - Design engineering population does not double every two years…
- Hence, a need for more efficient design methods
  - Exploit different levels of abstraction

Scaling Issues

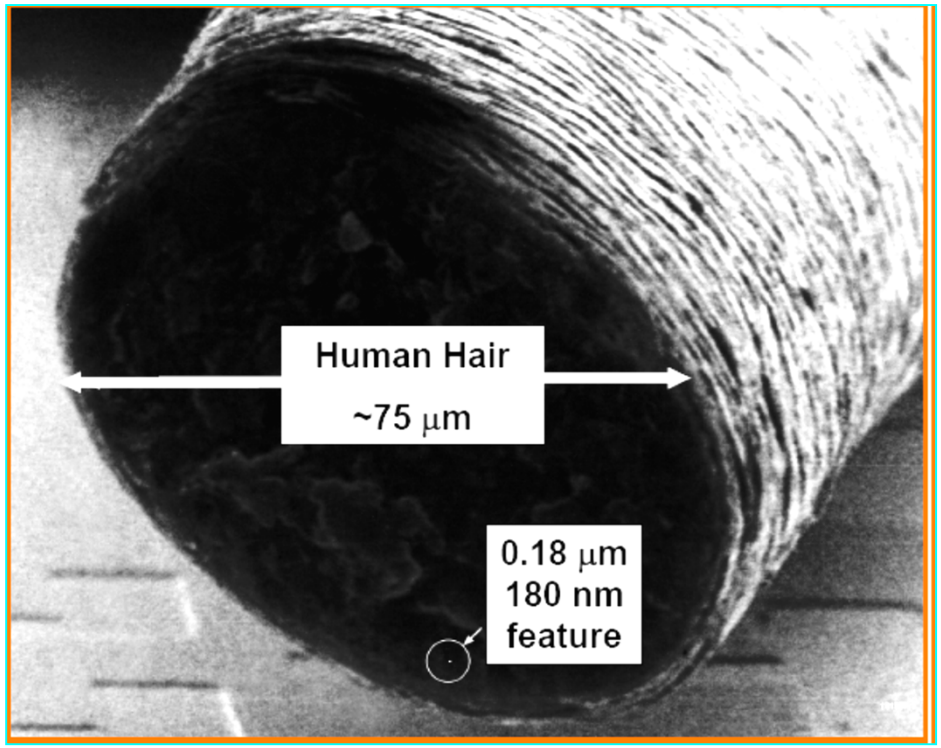




[Navakanta Bhat, 2007]

- SCE, High Leakage Current (Reducing L_g)
- Gate Leakage (Reducing t_{ox})
- High I_{off} (Reducing Voltage)

Fact findings to scaling



- Cross section of a single human hair can contain thousands of transistors !!!

- ~ 40,000 (65 nm node; L_G ~ 50 nm) transistors could fit on the cross – section of a hair.

ITRS Projections

Year of Production	2007	2010	2013	2016	2019	2020
Technology Node (nm)	65	45	32	22	16	14
Transistor Gate Length in Microprocessors circuits (nm)	25	18	13	9	6	5
Wafer diameter (inch)	12	12	18	18	18	18
Number of masks required for fabrication of Microprocessor	33	35	37	37	39	39
Number of Transistors in Microprocessor (billion)	1.1	2.2	4.4	8.8	17.7	17.7
Number of interconnect wiring levels in the Microprocessor	15	16	17	17	18	18
Number pins for packaged Microprocessor chip	1088	1450	1930	2568	3418	3760
Operating voltage (V)	1.1	1.0	0.9	0.8	0.7	0.7
Microprocessor frequency, GHz	9.3	15.1	23	39.7	62.4	73.1
Chip power dissipation (Watts)	189	198	198	198	198	198