EEE646 FPGA BASED SYSTEM DESIGN

Slot :G1+TG1

L	T	P	C
3	0	0	3

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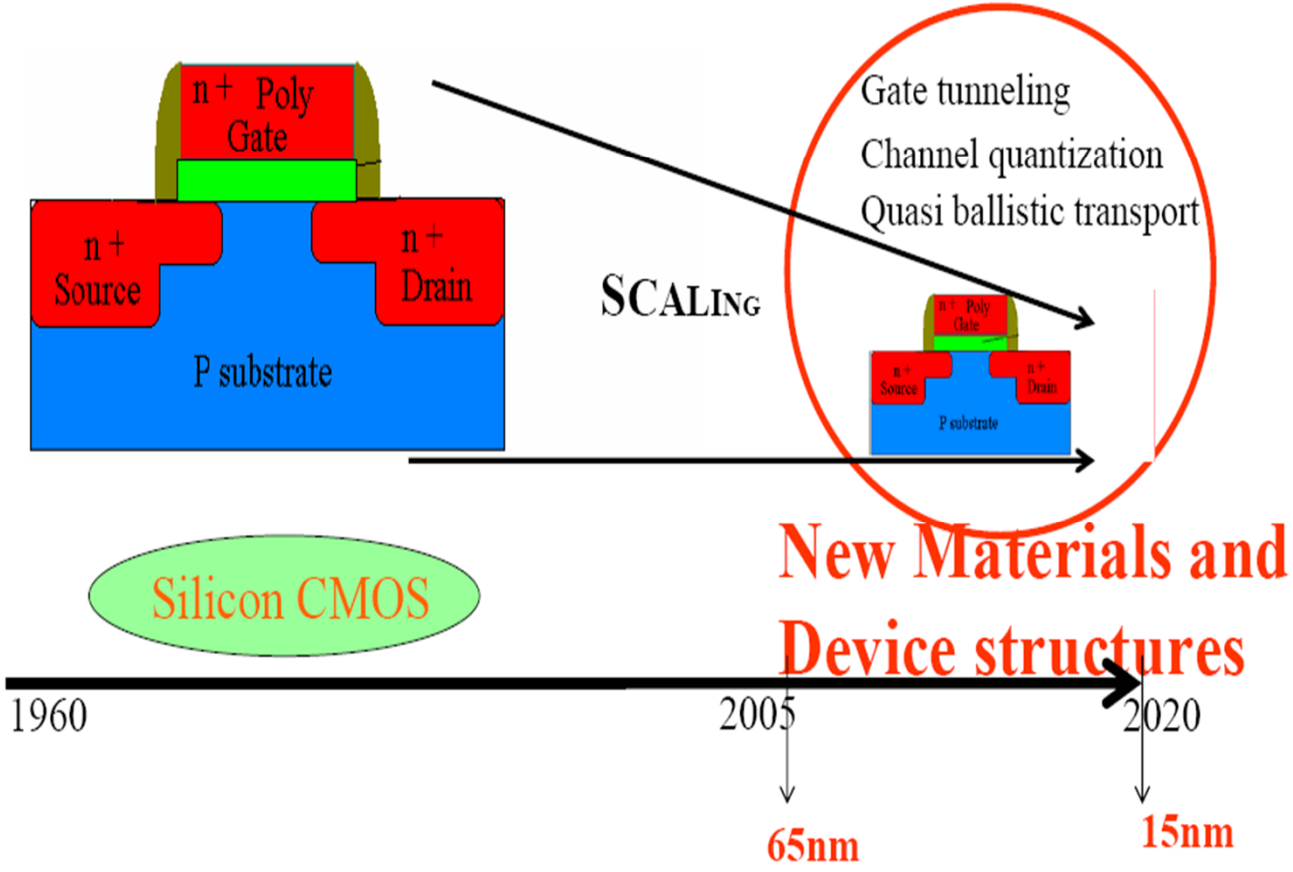
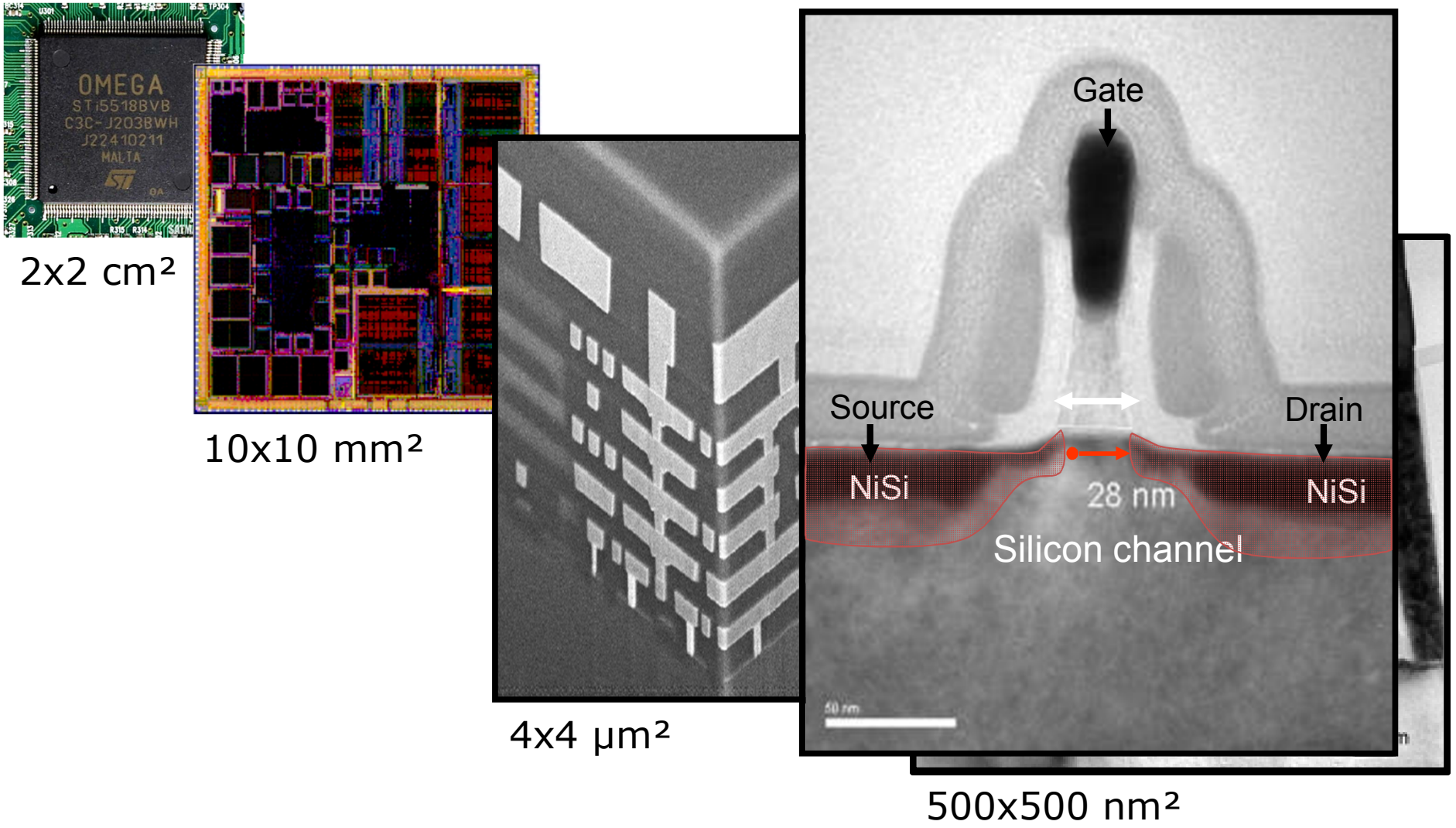
- Course Objective & Outcomes
- Syllabus
- Evaluation Procedure
- Integrated Circuit – An Overview & Evolution
- VLSI- Device Perspective
- VLSI-System Perspective
- Typical IC Design Flow
- Integrated Circuit Food Chain
- Discussion

VLSI- Device Perspective

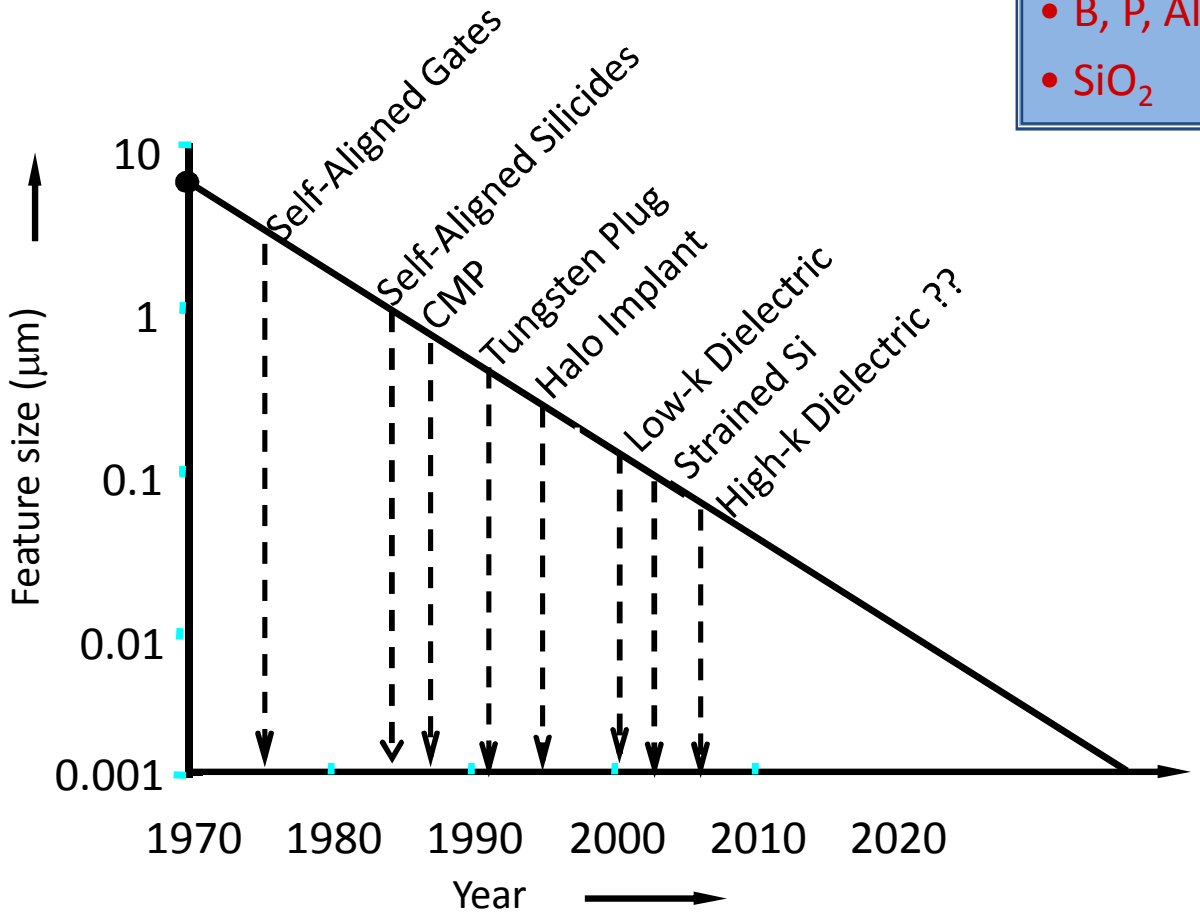
Microelectronics to Nanoelectronics



Different scales inside a chip



Technology is getting complex



1970

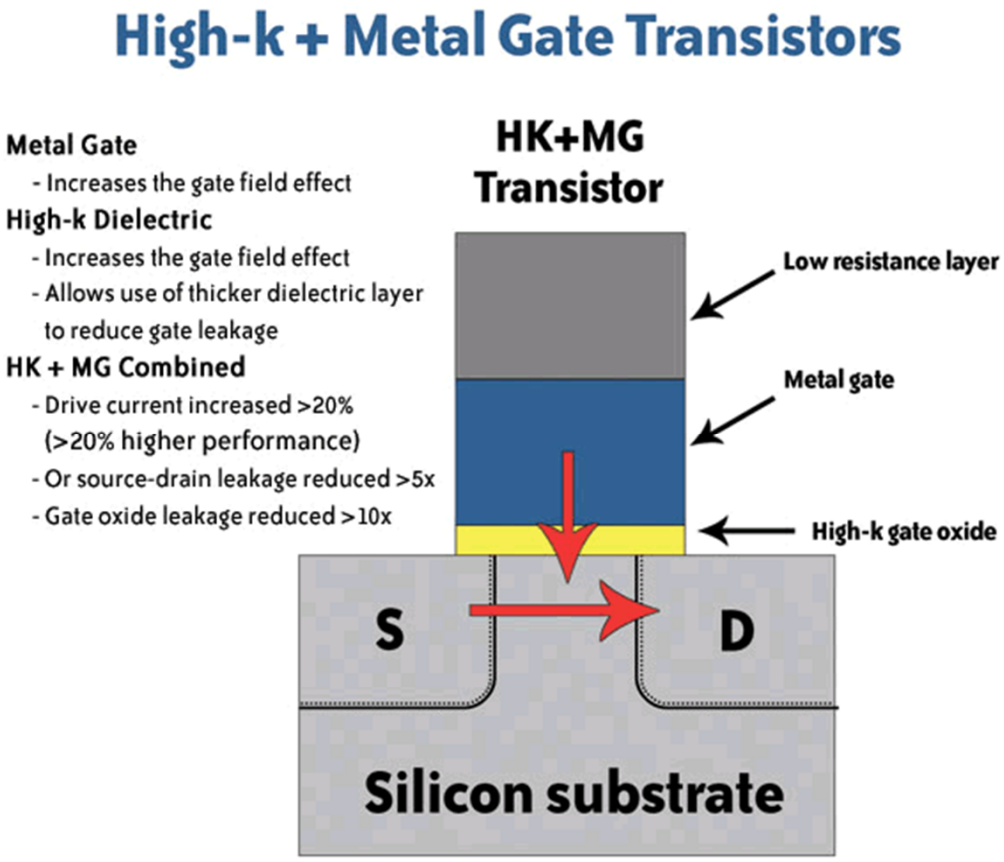
Si

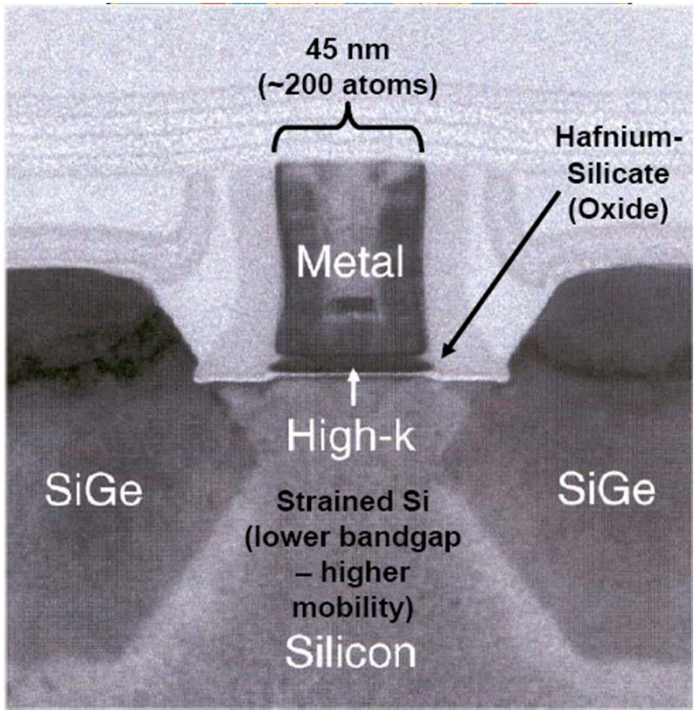
- B, P, Al
- SiO_2

2000

- SiGe
- Metal gates
- High-k dielectrics
- Low-k dielectrics
- Cu interconnects
- W plug
- Co-silicide
- Ti-silicide
- Ni-silicide
- Poly-Si
- Si_3N_4
- Oxi-nitride
- As, B, P, Al, SiO_2, Si.

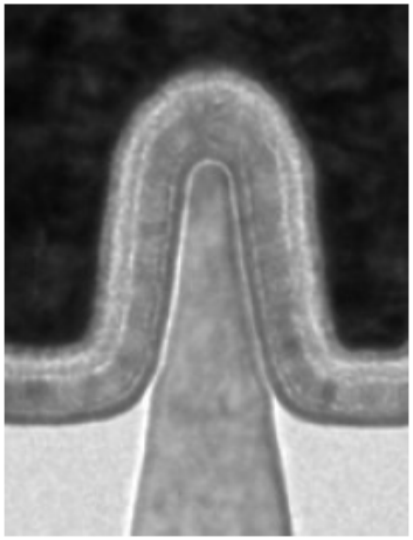
Intel's Transistor



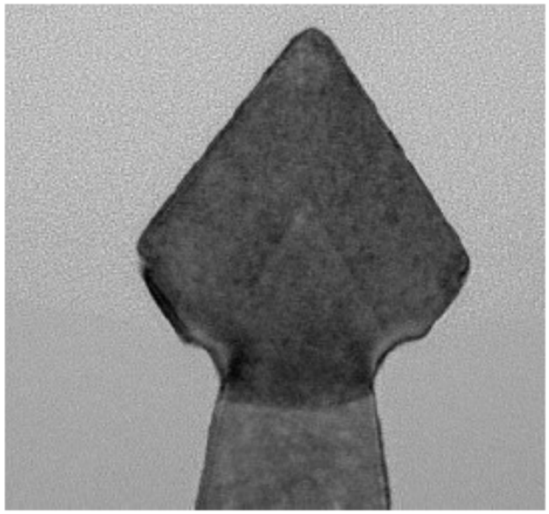


Intel's Transistor

C. Auth et al., pp.131, VLSI2012 (Intel)



PMOS channel under the gate

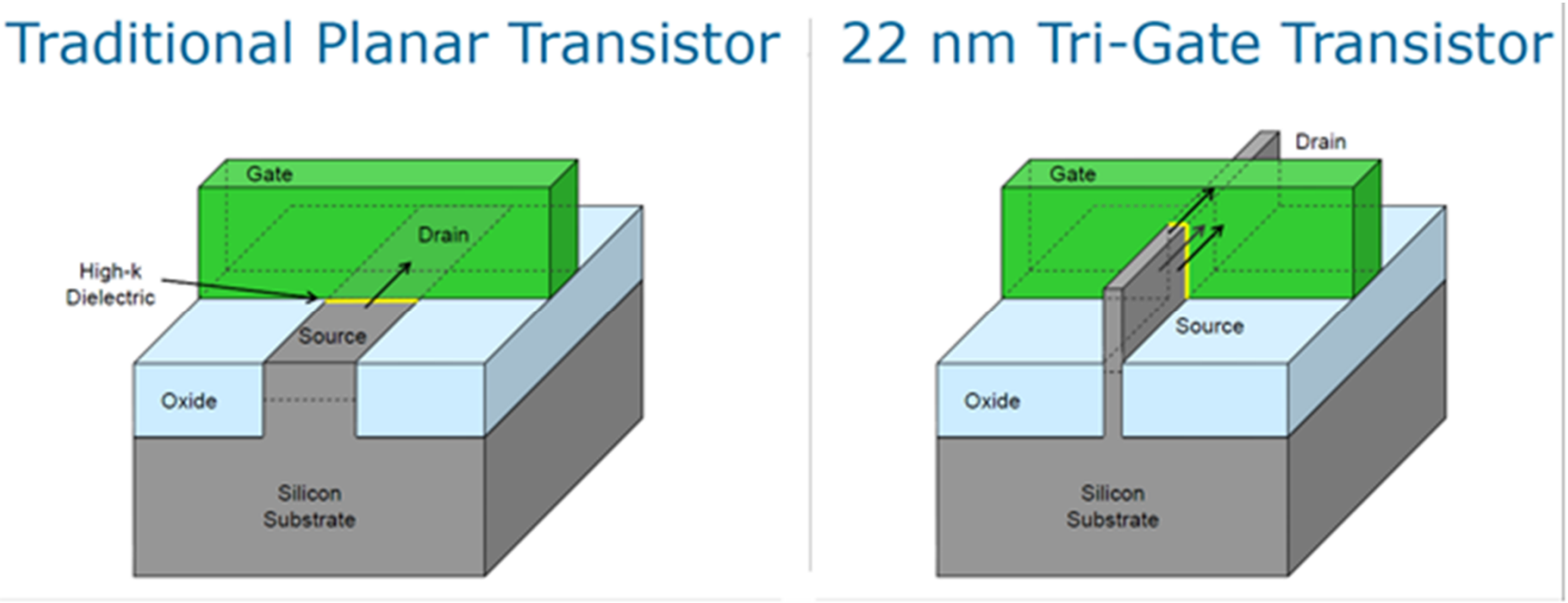


S/D region showing the SiGe epitaxy

A fin width of 8nm to balance SCE and R_{ext}

A fin height of 34nm to balance drive current vs. capacitance

3D Transistor



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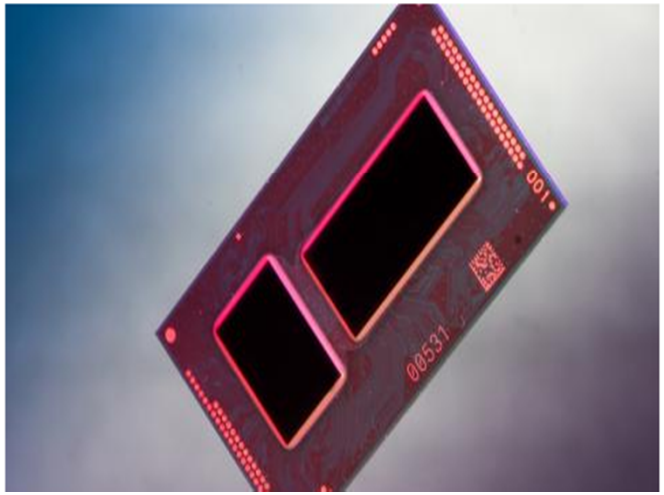
Intel® 14 nm Technology

Tags: Architecture & Silicon 14nm Process Technology

Ultra-fast, energy-sipping devices powered by Intel

Supporting a wide range of products from mobile devices to servers, 14 nm transistors improve performance and reduce leakage power. Intel® 14 nm technology will be used to manufacture a wide range of high-performance to low-power products including servers, personal computing devices, and products for the Internet of Things. The first systems based on the Intel® Core™ M processor were made available on shelves for the holiday selling season followed by broader OEM availability in the first half of 2015. Additional products based on 14 nm process technology will be introduced in the coming months.

Using 2nd generation 3D tri-gate transistors, the 14 nm technology delivers industry-leading performance, power, density, and cost per transistor, and will be



IBM's crazy-thin 7nm chip will hold 20 billion transistors

Looks like Moore's Law has some life in it yet, though creating a 7nm chip required exotic techniques and materials.

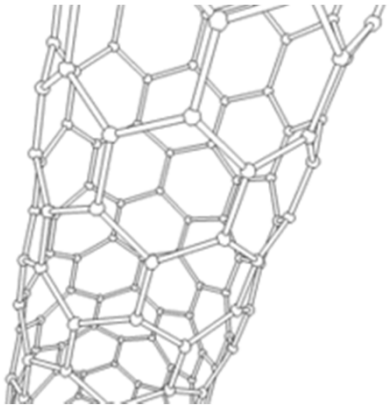
Brad Chacos | *@BradChacos*
Senior Editor, PCWorld

Jul 9, 2015 7:03 AM

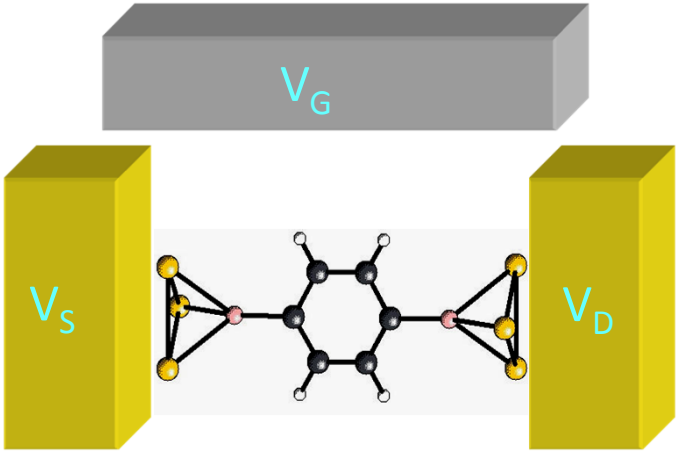
How far can we push Moore's Law? It's starting to become a concerning question as processors push into almost infinitesimally small process nodes.

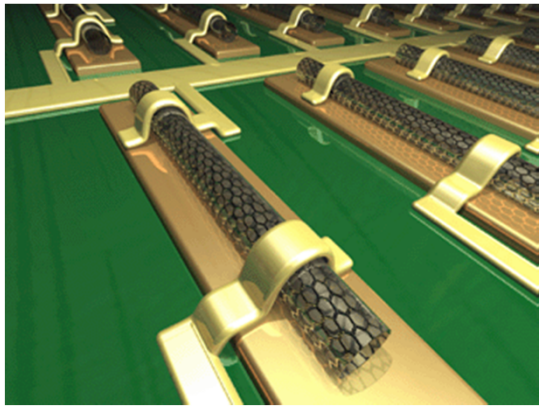
Intel's 14-nanometer Broadwell chips suffered from lengthy delays, stuttering Intel's vaunted tick-tock manufacturing schedule. TSMC, the company that manufactures graphics processors for AMD and Nvidia, has been stuck at the 28nm node for *years*

Future - nanoFET devices

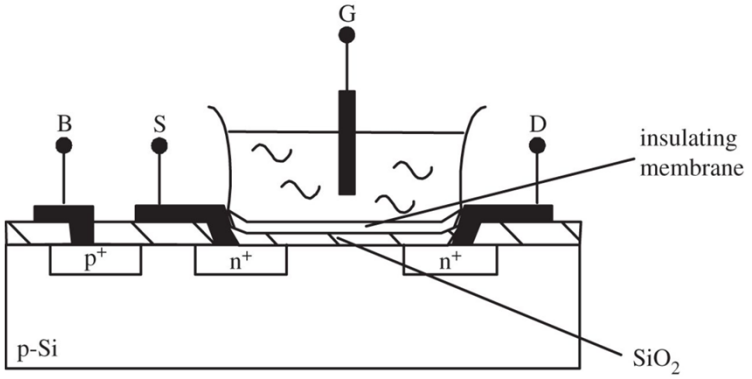


Molecular transistors.



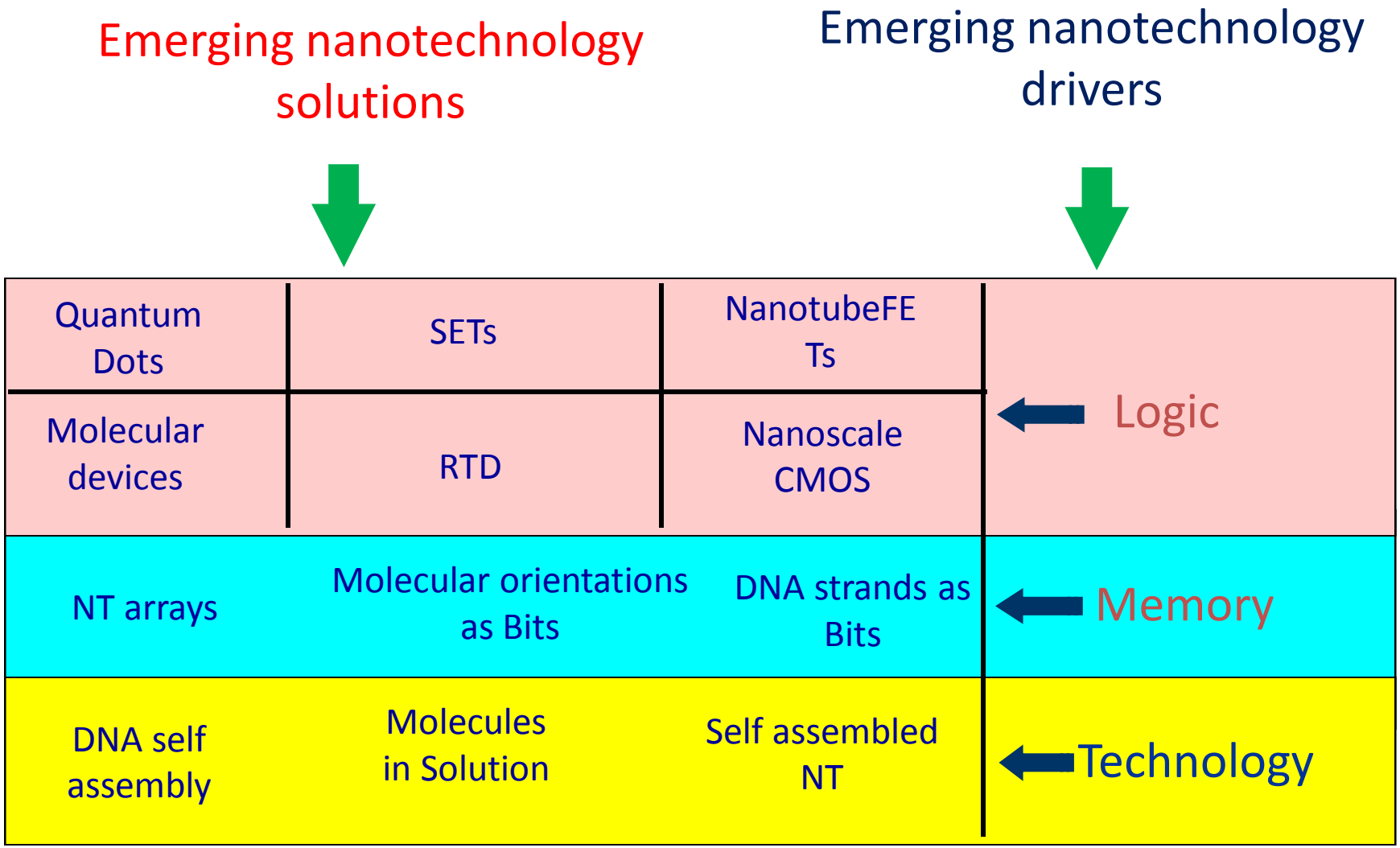


Ion- Sensitive Transistors



- Extensive modeling and comprehensive understanding are mandatory.

Alternatives to existing electronic systems



Performance parameters of a MOSFET

How can we categorize a MOSFET "good" or "bad"?

Threshold voltage (V_{th})	→	Lower
Off-state leakage current (I_{off})	→	Lower
On-state current (I_{on})	→	Higher
Transconductance (g_m)	→	Higher
Channel conductance (g_d)	→	Higher
Sub-threshold slope (S)	→	Smaller
Drain voltage (V_{dd})	→	Lower
Channel mobility (μ)	→	Higher
S/D resistance (R_s and R_d)	→	Lower
DIBL	→	Lower

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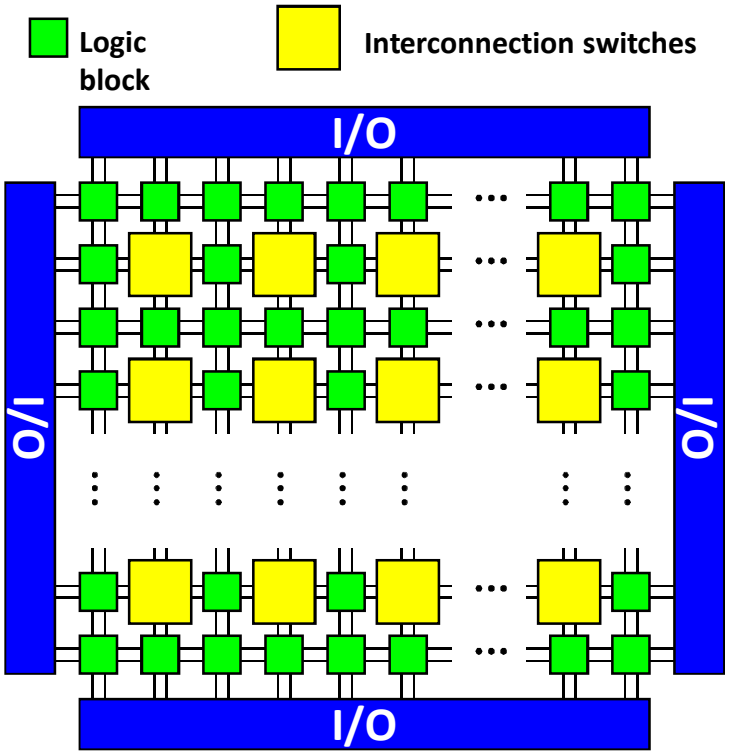
VLSI-System Perspective

ASIC

- Application **S**pecific Integrated Circuit
- E.g. Chip designed solely for use in cell phone
- A chip that can be designed by an engineer with no particular knowledge of semiconductor physics or semiconductor processes.

What is an FPGA?

- **Field Programmable Gate Array**
- Gate Array
  - Two-dimensional array of logic gates
  - Traditionally connected with customized metal
- Field Programmable
  - Field programmability is achieved through switches (Transistors controlled by memory elements or fuses)
  - One FPGA can serve every customer
- FPGA: re-programmable hardware



FPGA vs. ASIC

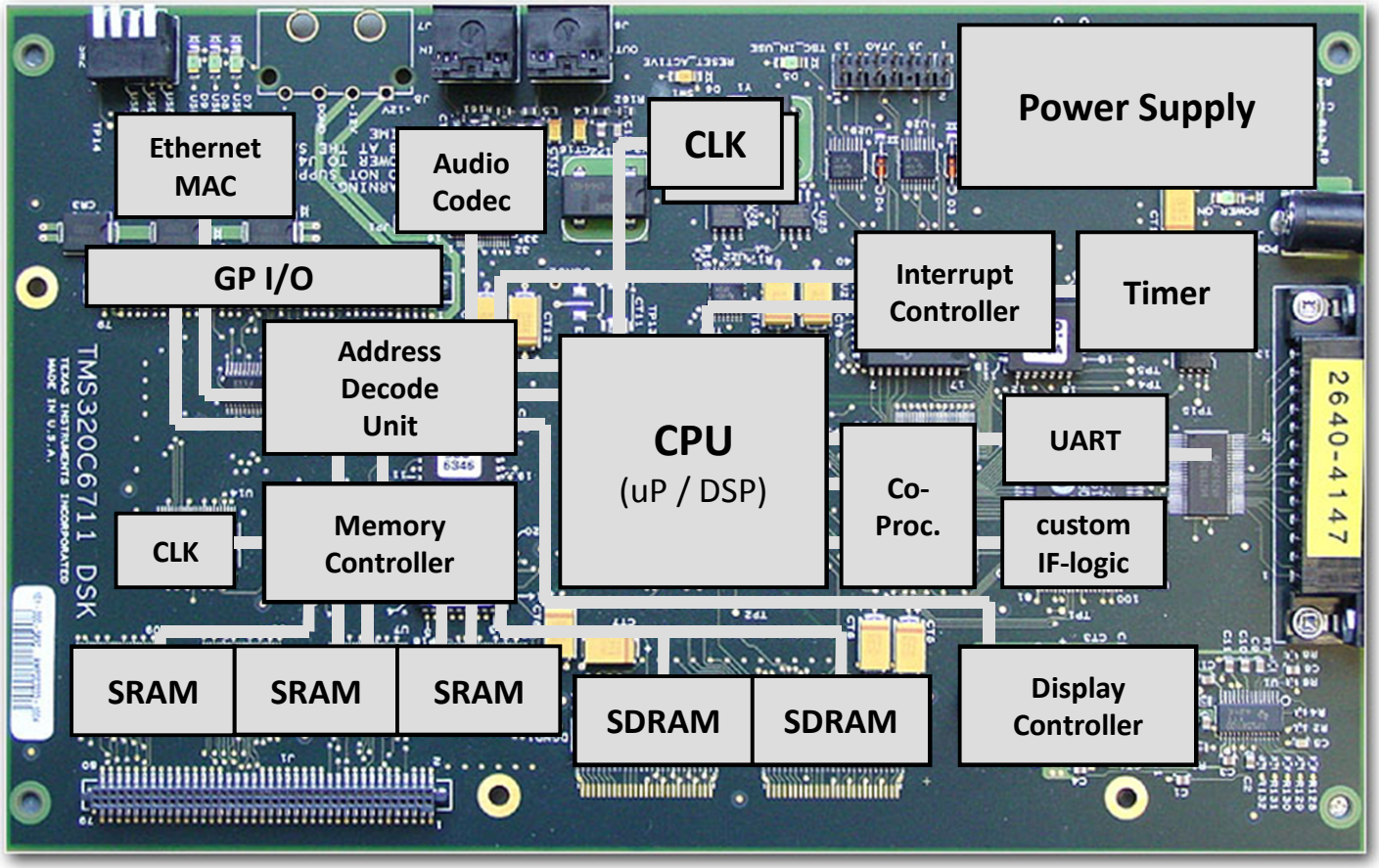
FPGA = Field Programmable Gate Array

flexibility of software + speed of hardware

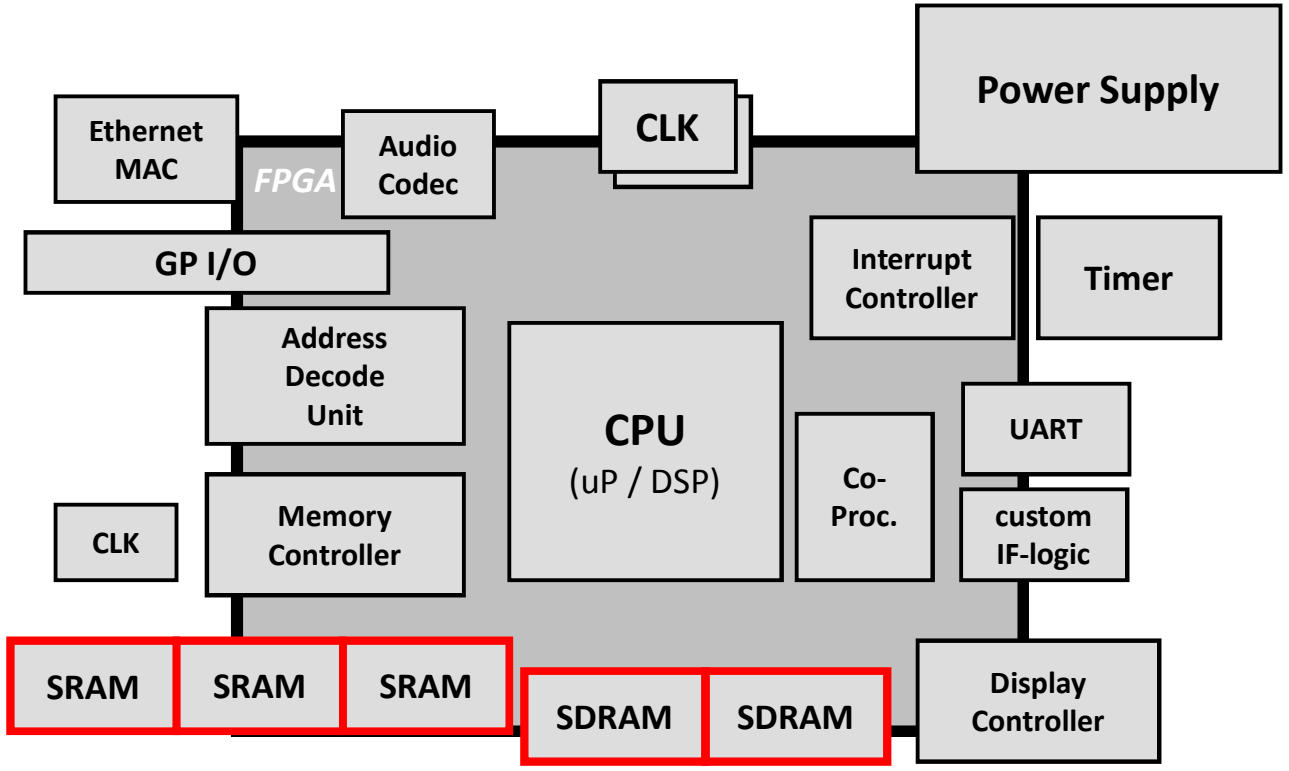
ASIC = Application Specific Integrated Circuits

CHARACTERISTIC	FPGA	ASIC
Time-to-market	Short	Long
High volume unit cost	High	Low
Flexibility after manufacturing	High	None
Performance	Medium	Very high
Density	Medium	Very high
Power consumption	High	Low
Minimum order quantities	None	High
Design flow complexity	Medium	Very high
Complexity of test	Low	High
Turnaround Time	Hours	Months

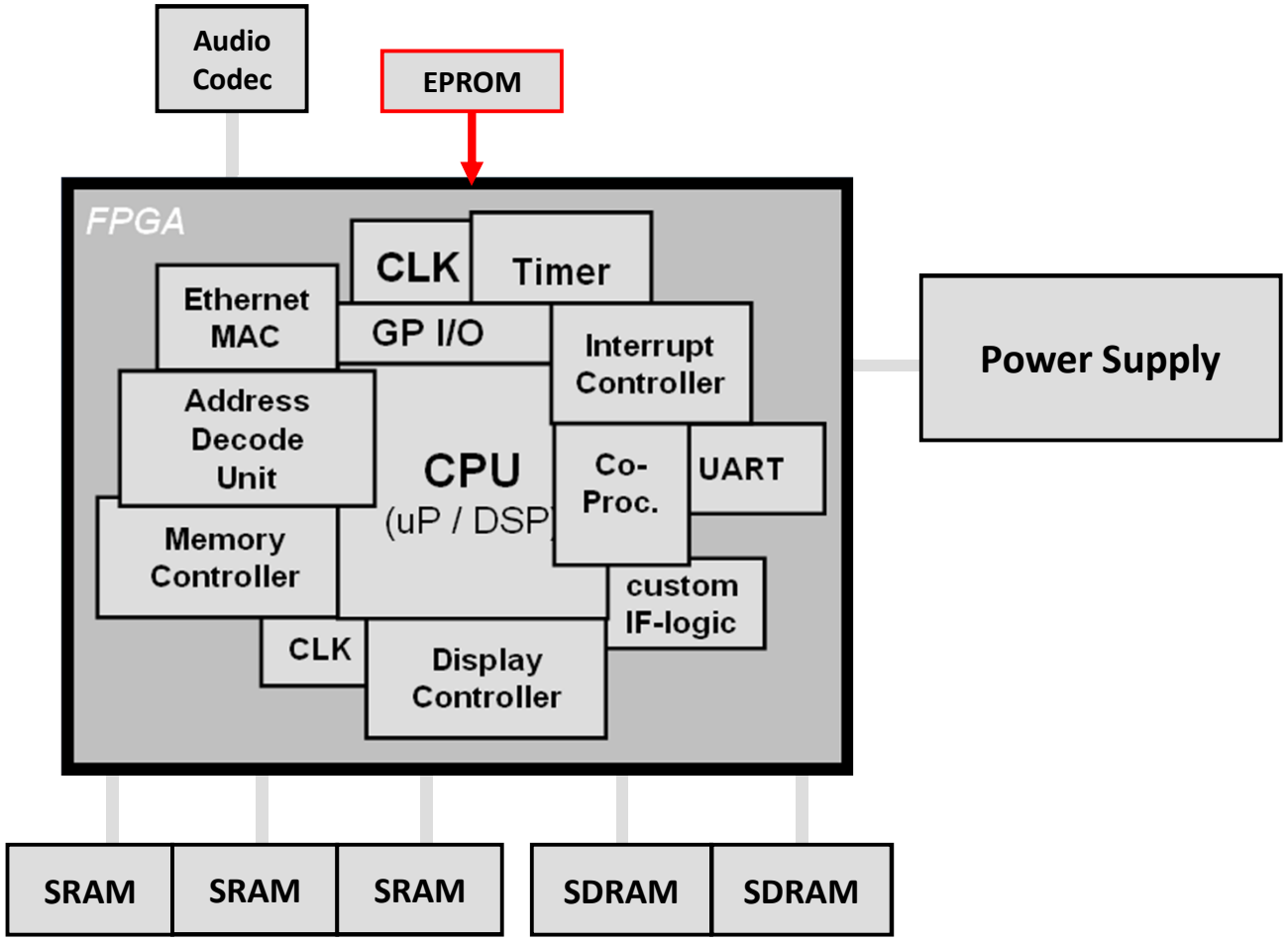
Traditional System Design



Next Step...


Power Supply
Ethernet MAC
Audio Codec
CLK
FPGA
GP I/O
Interrupt Controller
Timer
Address Decode Unit
CPU
(uP / DSP)
Co-Proc.
UART
CLK
Memory Controller
custom IF-logic
SRAM
SRAM
SRAM
SDRAM
SDRAM
Display Controller

Configurable System On Chip- CSoC



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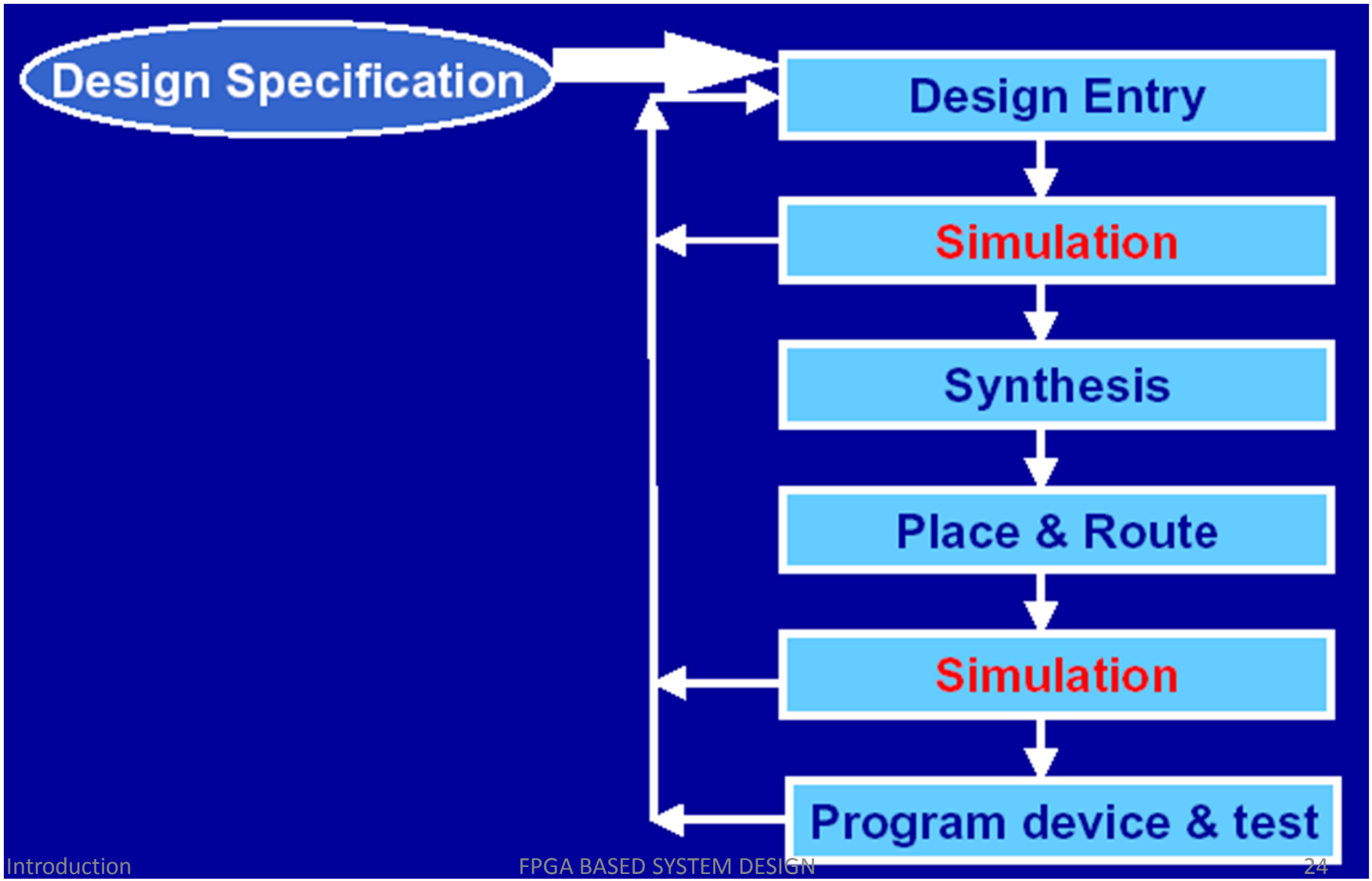
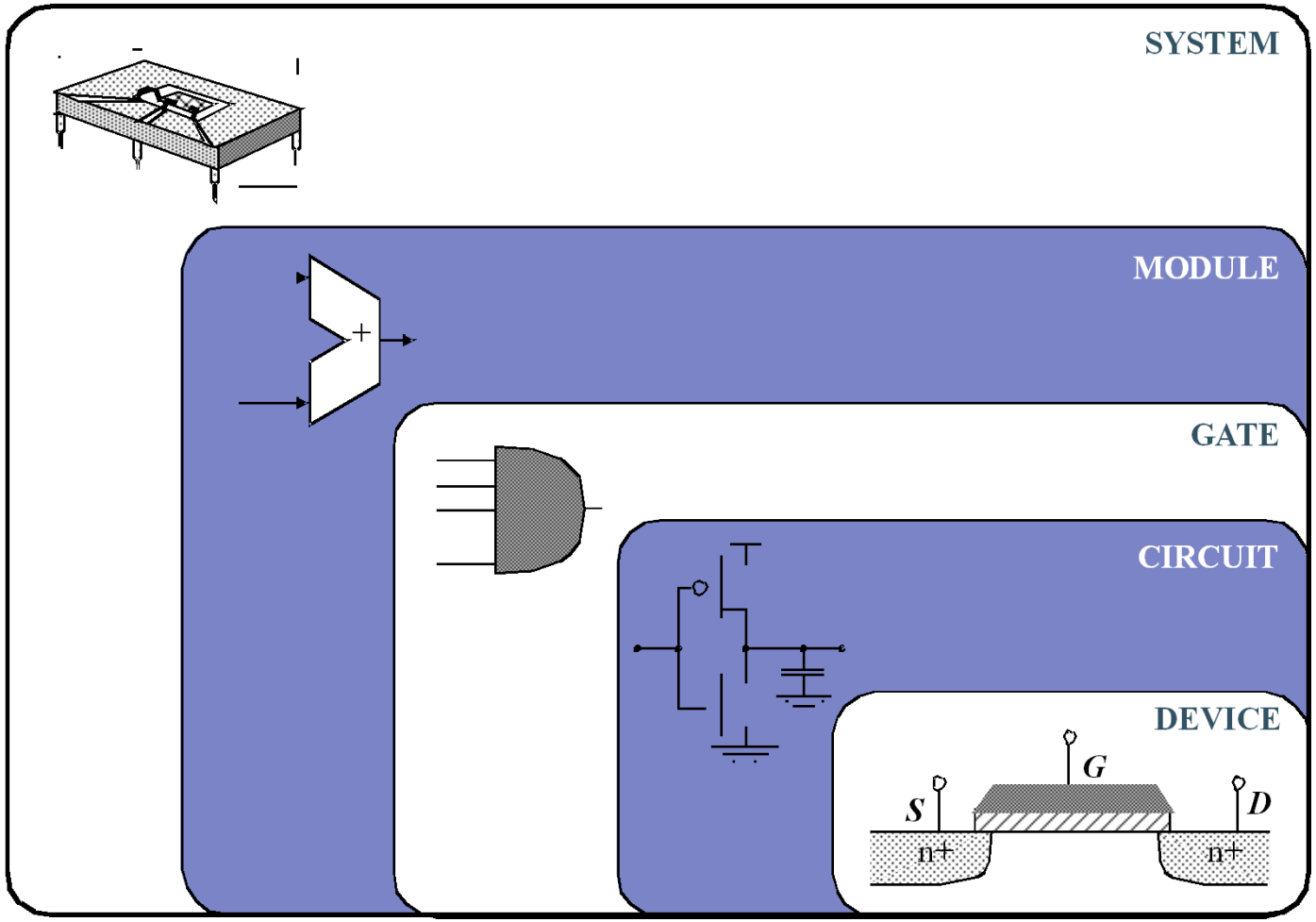
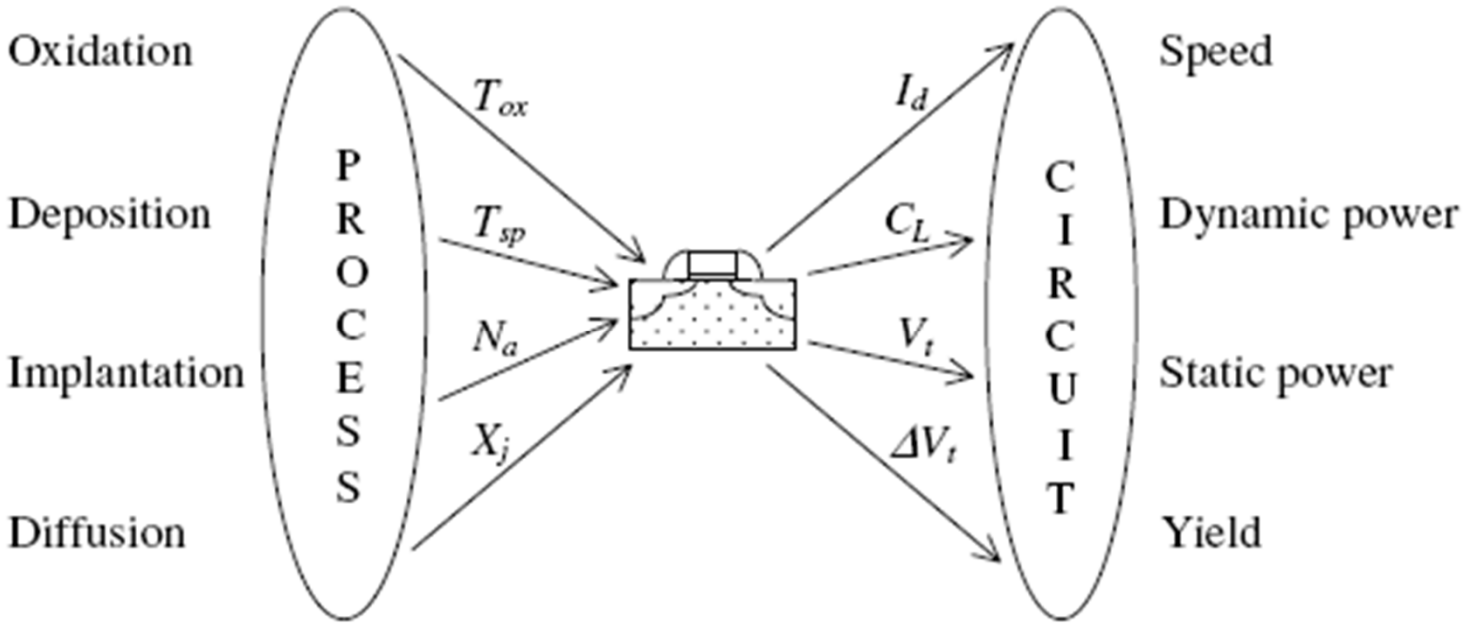
Typical Design Flow



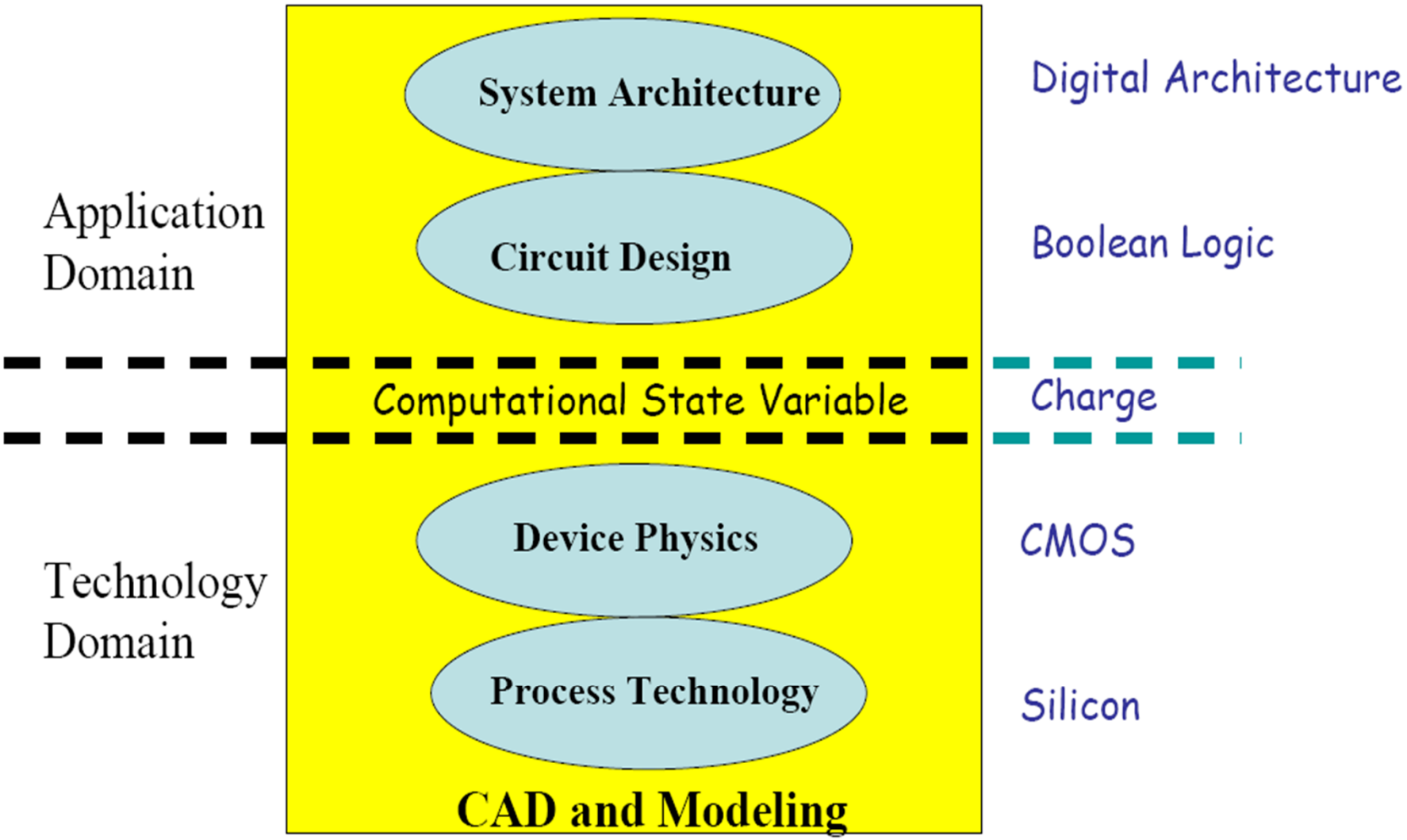
Design Abstraction Levels



Impact of device variability on circuit performance



The Integrated Circuit Food Chain



Optimization across all the domains is necessary