Evolution of CAD Tools & Verilog HDL Definition

K.Sivasankaran
Assistant Professor (Senior)
VLSI Division
School of Electronics Engineering
VIT University

Outline

- Evolution of CAD
- Different CAD Tools for IC Flow
- Emergence & Features of HDL
- VHDL Vs VerilogHDL
- Design Methodologies
- Verilog HDL – Definition
- Levels of Abstraction

Evolution of CAD

- The first Integrated Circuit (IC) or silicon chip was fabricated in 1960s.
- IC chip evolution -> SSI, MSI, LSI, VLSI…
- Designing single chip with more than 100,000 transistors - VLSI.
- Complicated design processes.
- Traditional / conventional design method includes manual translation of design description into logical equations and then to schematic.

Evolution of CAD

- Verification through bread-boarding?
- CAD (back-end) tools became critical.
- Graphic packages (PSpice, Workbench, OrCAD) for gate level / schematic representation.
  - –Cannot handle higher complexities.
  - –Poor portability.
  - –Poor readability for high complex designs.
- In all the above design methods the functional bugs cannot be identified till the design is implemented in hardware, and hence the design time is very long.

CAD for ASIC Design Flow

- Cadence
  - Digital, Analog and Mixed Signal, PCB Design, Testing and Verification.
- Synopsys
- Mentor graphics
- Magic

CAD for FPGA Design Flow

- Xilinx ISE and PAR , Partial Reconfiguration Flow
  - All Xilinx Devices
- ALTERA EDA Tools

  - All ALTERA Devices
- National Instruments

CAD Tools for Process and Device Simulation

- Synopsys TCAD
  - Sentaurus Process Simulator
  - Sentaurus Device Simulator
- Silvaco TCAD
  - Athena Process Simulator
  - Atlas Device Simulator

HDL?

- In electronics, a hardware description language or HDL is any language from a class of computer languages for formal description of electronic circuits. It can describe the circuit's operation, its design, and tests to verify its operation by means of simulation

- Popular HDLs are Verilog HDL & VHDL (for any complexity).

Emergence of HDLs

- High level languages such as FORTRAN, PASCAL, C, C++, etc., are sequential in nature.

- Digital designers felt the need for a standard language to describe digital systems / hardware.

- Hardware Description Languages (HDLs) comes into existence and these have special constructs to model the concurrency of processes found in digital systems.

Features of HDLs

- Easy development, verification and debugging through HDLs.
- HDL descriptions are easily portable, and is also compatible to all design tools.
- HDLs can describe the digital systems at various abstraction levels & also supports hierarchical modeling.
- HDL descriptions can be functionally simulated with Logic Simulators .

Features of HDLs

- Advent of Logic synthesis tools in late 1980's pushes HDLs to the forefront of digital design.

- Digital circuits described at Register Transfer Level (RTL) using HDLs, can also be synthesized through automated logic synthesis tools.

- Logic Synthesis tools can extract gate level details automatically from HDL (RTL) description.

VHDL Vs Verilog HDL

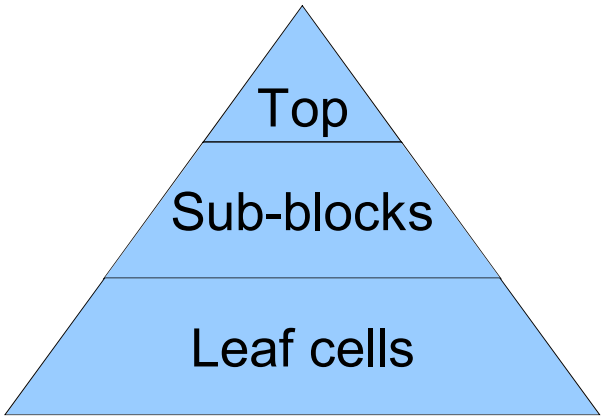
- VHDL : Very High Speed Integrated Circuit Hardware Description Language
- Verilog HDL: Verification Logic Hardware Description Language

Differences:

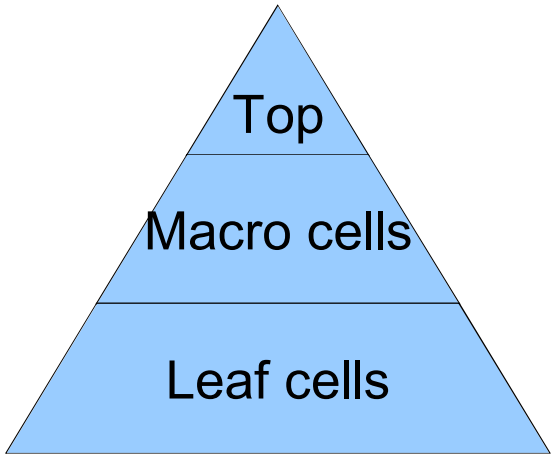
- VHDL was designed to support system level design and specification.
- Verilog HDL was designed primarily for digital hardware designers developing FPGAs and ASICs.

The differences becomes clear when one analyze the language features.

Design Methodologies



- Top-Down Design
  - Define the top-level block
  - Identify the sub-blocks necessary to build the top-level block
  - Sub-blocks are formed by leaf cells - the cells that can not be further divided



- Bottom-up Design
  - Build macro cells using leaf cells
  - Move up the hierarchy until the top-level is reached

What is Verilog HDL?

- Verilog HDL is a hardware description language used to design and document electronic systems.
- It allows designers to design at various levels of abstraction.
- It supports the development, verification, synthesis, and testing of hardware designs;.

Levels of Abstraction

- **Four Levels of Abstraction to represent the digital design**

Behavioral	The highest level of abstraction provided by Verilog HDL. A module is implemented in terms of the desired design algorithm
Data Flow	At this level the module is designed by specifying the data flow
Gate Level	The module is implemented in terms of logic gates and interconnections between these gates
Switch Level	This is the lowest level of abstraction provided by Verilog. A module can be implemented in terms of switches, storage nodes and the interconnections between them

Review

- Define HDL.
- Difference between HDL and HLL.
- Difference between VHDL and Verilog HDL
- Different design methodologies
- Different level of abstraction in verilog